REMARKS

As stated above, Applicants appreciate the Examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks. Applicants have carefully reviewed and considered the Office Action mailed on 17 October 17 2005, and the references cited therewith.

Presently, claims 1-20 are pending. Claims 6, 7, 11, 16 and 17 have been amended; as a result, claims 1-20 are still pending in this application.

In the subject action, the Examiner rejects claims 5-8 and 15-18 under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner appears to suggest that Figure 1 and the specification of the subject application do not disclose that the overhead extractor may provide encoded bits in parallel.

Figure 2 of the subject application is reproduced below and includes an overhead extractor interface 108. Outputs signals 115, 116, 117 and 118 are provided by overhead extractor interface 108. At least one of these output signals may include binary data that may be output in a parallel manner. In particular, receive overhead data signal 116 may provide output data in parallel.

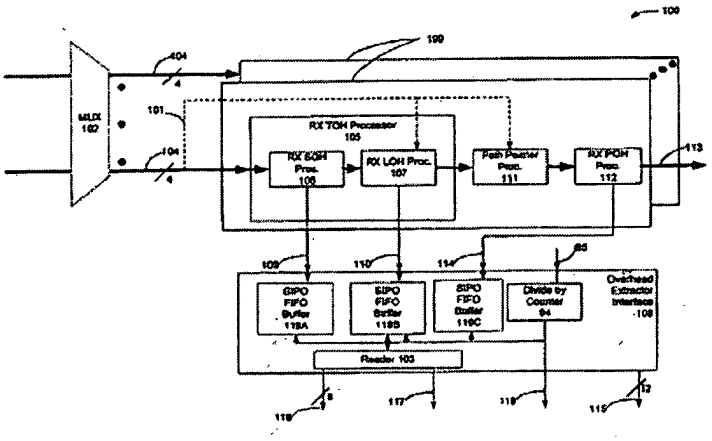

Figure 2

Outputting of receive overhead data signal 116 in a parallel manner is described in paragraphs 0026 and 0027 of the subject application, as follows:

> [0026] Processed overhead information from overhead extractor interface 108 is provided as receive overhead address signal 115, which is generated and formatted as described below, receive overhead data signal 116, receive overhead parity signal 117 and receive overhead clock signal 118. For purposes of clarity a 16 channel STS-3 input exemplary embodiment is described. However, fewer or more channels, as well as fewer or more STS levels, may be used in accordance with one or more aspects of the present invention. Receive overhead address signal 115 is 12 bits wide, receive overhead data signal 116 is eight bits wide, receive overhead parity signal 117 is one bit wide, and receive overhead clock signal is one line. Accordingly, 22 separate lines are provided from overhead extractor interface 108 to provide signals 115 through 118. Notably, fewer or more bits may be used to provide receive overhead address signal 115.
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> [0027] TOH and POH overhead bytes, namely, all overhead bytes in a frame, of channels 104 are output in parallel as receive overhead data signal 116, which is one byte wide. Continuing the example of an STS-2 frame for purposes of clarity, there are nine rows and nine columns of TOH in an STS-3 frame. Additionally, there are nine rows and three columns of POH in an STS-3 frame. To uniquely identify a channel number and a location of each overhead byte in an STS-3 frame, a 12-bit addressing scheme is employed for this example with 16 channels. This addressing scheme is reflected in receive overhead address signal 115. Other addressing schemes may be used as long as each byte, frame and channel are uniquely identified.

Thus, at least one output signal of the overhead extractor (e.g., receive overhead data signal 116) may be output in a parallel manner. For at least this reason, Applicants respectfully assert that Figure 2 and the specification disclose that encoded bits may be provided in a parallel manner from the overhead extractor. Accordingly, Applicants respectfully assert that claims 5-8 and 15-18 are patentable and the rejection should be withdrawn.

Also in the subject action, the Examiner rejects claim 20 under 35 USC §112, second paragraph as being incomplete for omitting essential elements and steps. In particular, the Examiner appears to suggest that a line overhead processor element has been omitted from the claim.

Applicants are confused by the Examiner's rejection. Claim 20 requires that a first overhead portion includes Section Overhead and a second overhead portion includes Path Overhead. Applicants respectfully assert that overhead portions may include Section Overhead

and/or Path Overhead as described in paragraph 0004 of the subject application. Reciting paragraph 0004 of the subject application:

> [0006] Referring to FIG. 1, there is shown a block diagram of an exemplary embodiment of Synchronous Transport Signal (STS) frame 10 in accordance with the prior art. STS frame 10 may be any of a variety of levels, conventionally where N is equal to 1, 3, 12, 48, 192, or 768 and data rate is N times 51.84 megabits per second (Mbps); although, N may be an integer coventionally from 1 to 768. As shown in FIG. 1, an STS-3 frame 10 is indicated. Frame 10 comprises section overhead (SOH) 18, line overhead (LOH) 19, and in payload area 12 comprise path overhead (POH) 15 and user data area 14 both of synchronous payload envelope (SPE) 13. STS-3 frame 10 may be provided on a separate channels. So, continuing the above example, STS-N may be channelized. (emphasis added)

Accordingly, Applicants respectfully assert that claim 20 is patentable and the rejection should be withdrawn.

Also in the subject action, the Examiner rejects claims 6-8 and 16-18 under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner appears to suggest that the term "the overhead processor" is not clear as there are three overhead processors included in the system.

Claims 6, 7, 16 and 17 have been amended to clarify the overhead processor as the first overhead processor.

Also in the subject action the Examiner objects to claim 11 for informality. In particular, the Examiner appears to suggest the term "the overhead processor" lacks proper basis.

Independent claim 11 has been amended to provide proper antecedent basis.

Turning to the rejections on the art, claims 1-20 stand rejected under 35 USC §102(b) as being anticipated by Huscroft et al. (U.S. Patent No. 5,568,486; hereinafter Huscroft).

The Examiner points to Huscroft as disclosing an integrated user network interface device that includes: a section overhead (SOH) processor 22 to process section overhead portion (a first overhead processor coupled to the at least one channel and configured to obtain a first portion of transport information); a line overhead (LOH) processor 26 to process line overhead portion (a second overhead processor coupled to the at least one channel and configured to obtain a second portion of transport information); a path overhead extract 56 to identify POH

location (RPOHFP: receive path overhead frame position) in the SONNET frame (a path pointer processor); and a path overhead (POH) processor 28 to process path overhead portion of a SONET frame (a third overhead processor coupled to the path pointer processor and configured to obtain a third portion of transport information). The Examiner further points to Huscroft as disclosing a transport overhead extract 54 coupled to the SOH processor 22, LOH processor 26 and POH processor 28 (an overhead extractor coupled to the first overhead processor, the second overhead processor and the third overhead processor to receive the first portion of transport information, the second portion of transport information and the third portion of overhead). The Examiner points to Huscroft as disclosing that the transport overhead extract 54 encodes to provide a receive transport overhead frame position (RTOHFP, col. 10, lines 49-52), and inherently encodes SOH and LOH portions of the SONET frame to provide frame (byte A1 and A2) and channel (byte D1-D12) information (the overhead extractor configured to encode the first portion of the overhead and the second portion of the overhead and to provide a field of encoded bits representative of a frame number, a channel number and an overhead byte location).

The Examiner appears to assert that Huscroft teaches "an overhead extractor coupled to a first overhead processor and a second overhead processor to receive a first portion of overhead and a second portion of overhead", as required by independent claim 1. To provide this limitation, the Examiner appears to assert that Receive Transport Overhead Extract Port 54 (shown in FIG. 5 of Huscroft) is coupled to section overhead (SOH) processor 22, receive line overhead (LOH) processor 26, and receive path overhead (POH) processor 28. However, Huscroft does not disclose or suggest that processors 22, 26 and 28 are coupled to Receive Transport Overhead Extract Port 54. In contrast, Huscroft discloses that just one of the processors is involved with extracting overhead data. In particular, Huscroft describes that only receive path overhead processor 28 provides overhead extraction. In this regard Huscroft discloses:

> "Referring to FIG. 5 there is shown the user network interface device 10 which consists of a parallel/serial transmit circuit 18 and a serial/parallel receive circuit 20. Transmit circuit 18 transmits SONET/SDH frames, via bit serial or byte serial signals and receive circuit 20 receives such frames in bit serial or byte serial format. Received bit serial signals are converted by the user network interface device 10 to byte serial format.

> The output of the receive circuit 20 is coupled to the input of a receive section overhead processor 22 which provides frame synchronization, de-scrambling, section level alarm and performance monitoring. The output of the receive section overhead processor 22 is coupled to the input of a receive line overhead processor 26 which provides line level alarm and performance monitoring. The output of the line processor 26 is connected to the input of a receive path overhead processor 28 which provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (SPE), and path level alarm and performance monitoring.
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> Once SONET/SDN overhead processing is complete the signals from the output of the receive path overhead processor 28 are directed to the input of a receive ATM cell processor 30. The ATM cell processor 30 performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The output of the receive ATM cell processor 30 couples to the input of a 4 cell deep receive FIFO 32 which passes data structures consisting of either 27 16-bit words, or 53 8-bit words and is used to separate the STS-3c line timing from the higher layer ATM system timing. The output of the FIFO couples to the input of a drop side interface 34." (emphasis added) (col. 6, line 53 to col. 7, line 18)

In contrast, Applicants' independent claim 1 requires "an overhead extractor coupled to a first overhead processor and a second overhead processor to receive a first portion of overhead and a second portion of overhead..." Thus, the overhead extractor is coupled to at least two overhead processors and receives overhead from both overhead processors. Applicants' invention of independent claim 11 requires similar limitations.

As described above, Huscroft is understood to disclose a single overhead processor (i.e., receive path overhead processor 28) for extracting overhead and not two or more overhead processors that provide overhead extraction. Thus, since the limitations of Applicants' independent claims 1 and 11 are not disclosed or suggested in Huscroft, Applicants respectfully submit that Huscroft could not anticipate Applicants' invention of claims 1 and 11. The remaining claims of this rejection depend directly or indirectly upon Applicants' invention of independent claims 1 and 11, and thus must be read as incorporating the limitations of the respective independent claims. (35 USC §112, 4th paragraph). Since nowhere does Huscroft disclose or suggest these limitations of claims 1 and 11, it is respectfully submitted that the Examiner's rejection of claims 2-10 and 12-20 as being anticipated by Huscroft is in error, and should be withdrawn.

Having dealt with all the objections raised by the Examiner, it is respectfully submitted that the present application, as amended, is in condition for allowance. Thus, early allowance is earnestly solicited. The Examiner is invited to telephone Applicants' attorney (603-668-6560) to facilitate prosecution of this application.

In the event there are any fees due, please charge them to our Deposit Account No. 50-2121.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17 day of January, 2006.

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Name

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Signature